Instrument FSW - Approach/Review

9/19/2001
Near Term Activities

- Decision to allocate the Instrument processor related HW and SW control functions to the FAME Spacecraft Controller was made 9/5/2001

- This package summarizes the activities and outlines pre-PDR plans related to the decision.

- Enlist program support wherever possible to accomplish pre-PDR objectives.
Primary Objectives Prior to PDR

• Bus/Instrument Interface Definition

• Capture of Overall Instrument FSW Requirements

• Algorithm Selection

• Processor Throughput Analysis and Test

• Software Team Organization and Development Plan

• High Level Design

• Instrument Test Approach
Bus/Instrument Interface Definition

- Resources to date:
  - Primary discussions have been between LM ATC (Earl Aamodt, Peter Ogden and Mike Wagner) and NRL (Brian Davis and John Gambert)
  - Additional review feedback has been received from others at NRL, LM ATC and USNO

- Activities to Date:
  - For the last two weeks, almost daily review and definition discussions have taken place.

- Products to Date:
  - Bus/Instrument Interface Review Package (powerpoint)

- Plans:
  - Continue using review package until interface stabilizes and then transfer the information to the Bus/Instrument ICD (Hardware).
Capture of Overall Instrument FSW Requirements

- **Resources to Date:**
  - Instrument Requirement Document (IRD), 22-May Draft
  - Discussions with Dave Fish and Chin-an Cheng

- **Activities to Date:**
  - Reviewed IRD

- **Products to Date:**
  - None

- **Plans:**
  - Capture requirements into the Observatory FSW requirements specification
    - Will contain combined Bus and Instrument FSW requirements
  - Utilize NRL, LM ATC and USNO personnel to review and refine, as needed, the Instrument FSW requirements
  - Perform a Program level review of the FSW requirements prior to PDR
    - Schedule TBA
Algorithm Selection

- Resources to Date:
  - Technical Memos (Rob Olling, George Kaplan, Roel Vanbeezooijen)
  - E-mail/Attachments from Algorithm Working Group members
  - Draft Template of the Algorithm Description Document (ADD)

- Activities to Date:
  - Discussed algorithm status and approach with Roel and Dave Fish
  - Distributed draft template of the ADD

- Products to Date:
  - None

- Plans:
  - Work a plan during the TIM to complete a full draft of the ADD prior to PDR
  - Seek ongoing support from the Algorithm Working Group members (and others) to review and refine the ADD
  - Schedule telecons, as required, to support ADD development
  - Utilize prototype code development, where necessary, to support algorithm assessment and selection.
Processor Throughput Analysis and Test (1 of 2)

• Resources to Date (From Dave Fish, Bob Drake and Chin-an Cheng):
  - Notes
  - Presentation Material
  - Estimations
  - Measured and scaled results from prototype code
  - Prototype source code and star catalog data files

• Activities to Date:
  - Discussed throughput analysis status with Dave Fish
  - Currently in the process of obtaining prototype source code and data files (i.e. star catalog) from LM ATC - Dave Fish, Chin-an Cheng and Bob Drake are supporting this effort.
  - LM ATC is in the process of providing additional description and documentation in support of the prototype code and data files
  - NRL FSW team is preparing FSW development environment to support the adaptation of the existing prototype code for execution on the RHC-3001 target

• Products to Date:
  - FAME application is being prepared to support Instrument FSW prototype code integration
  - FSC engineering unit is ready to support FSW prototype code execution using a partial Star Catalog
Processor Throughput Analysis and Test (2 of 2)

• Plans:
  - Refine Bus and Instrument processor throughput requirements
  - Use available RHC-3001 based FAME Bus application (RM & CT) and existing ICM Application (RM, CT & ADAC) to obtain a Bus processing throughput estimate.
  - Adapt key portions of the Science Data collection prototype code to the VxWorks and RHC-3001 environment to obtain Science Data collection processing throughput estimate.
  - Coordinate these efforts with the activities of the Algorithm Working Group members and the ongoing development of the ADD.
  - This effort is both dependent on the algorithm selection, but can provide feedback relating to algorithm efficiency.
  - Continue to coordinate with LM ATC team to utilize their experience with prototype implementations and utilize their prototype development and execution environment (w/support form Roel, Dave & Bob).
Software Team Organization and Development Plan

• Resources to Date:
  - LM ATC FSW and System Engineering Team
  - NRL FSW Team
  - Enlisted help from Bob Stapleford and Jim VanGaasbeck to provide added Pre-PDR (and post-PDR) Instrument FSW system engineering support
  - Existing Bus and Instrument Flight SW Development Plans

• Activities to Date:
  - Discussed LM ATC Flight SW activity, requirements, design and prototype status with LM ATC FSW team

• Products to Date:
  - None

• Plans:
  - Discuss pre and post PDR FSW team organization approaches with NRL and LM ATC management (during the TIM)
    - Decide on pre-PDR team organization ASAP (during TIM)
    - Work on long term (post-PDR) team organization and integration issues - initial plan by 9/28
  - Generate a draft Observatory Flight SW Development Plan prior to PDR - balance budget constraints, available resources, development approach with risks
High Level Design (PDR preparation)

- Resources to Date:
  - LM ATC IPDR package
  - Existing FSW requirements (IRD)
  - LM ATC FSW team support

- Activities to Date:
  - Reviewed existing material

- Products to Date:
  - None

- Plans:
  - Design decisions will be based on:
    - Existing design approach from LM ATC
    - Results from combined requirements
    - Algorithm Selection
    - Processor throughput analysis and test results
    - Integration approach of instrument functionality with FAME application (ICM based)
  - Some key decisions
    - Full redundancy (Full Bus/Instrument functionality on a single processor) or Distributed Processing (Bus/Instrument functionality distributed across two processors with degraded capability in the presence of a processor failure)
    - Explore options with respect to requirement allocation between flight and ground processing
      - Investigate feasibility of utilizing ground processing assets for acquisition and/or fine attitude/rate determination
Instrument Test Approach - From a control and data standpoint

- **Resources to Date:**
  - LM ATC IPDR package
  - USNO, LM ATC and NRL personnel

- **Activities to Date:**
  - Reviewed some material

- **Products to Date:**
  - None

- **Plans:**
  - Develop an integrated program approach to testing in light of the processor allocation
    - Organize and define a plan to document test approach during the TIM (9/20)
  - Identify test and calibration requirements, HW & SW requirements and a high level schedule associated with each of the following activities:
    - Instrument Standalone testing
    - FSW Standalone testing
    - Integration of Bus CT&DH (HW & SW) with the Instrument at LM ATC
    - Observatory integration at NRL
    - On-Orbit test and calibration activities